**ISA Specifications** :-

* **Instruction width :** 12 bits
* **No of operands :** 3, each consisting of 3 bits
* **No of Formats:** 3; R-Type, I-Type, J-Type
* **No of instructions :** 8
* **List of instructions with instruction type:-**

| Arithmetic | Logical | Transfer | Jump |
| --- | --- | --- | --- |
| ADD,SUB, ADDi | AND, XOR | LW,SW | JUMP |

**Register Table** :-

| Register Number | Value | Name |
| --- | --- | --- |
| 0 | 0 | $r0 |
| 1 | 1 | $r1 |
| 2 | 10 | $r2 |
| 3 | 11 | $r3 |
| 4 | 100 | $r4 |
| 5 | 101 | $r5 |
| 6 | 110 | $r6 |
| 7 | 111 | $r7 |

**Formats:-**

R-type

| 3 bit | 3 bit | 3 bit | 3 bit |
| --- | --- | --- | --- |
| opcode | Rd | Rs | Rt |

I- type

| 3 bit | 3 bit | 3 bit | 3 bit |
| --- | --- | --- | --- |
| opcode | Rd | Rs | Immediate |

J- type

| 3 bit | 9 bit |
| --- | --- |
| opcode | Target |

**Instruction Table:-**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Opcode | Format Type | Example | Meaning |
| add | 0 | R | add r1 r2 r3 | r1 = r2 + r3 |
| sub | 1 | R | sub r1 r2 r3 | r1= r2 - r3 |
| addi | 10 | I | addi r1 r2 5 | r1 = r2 + 5 |
| lw | 11 | I | lw r1 r2 5 | r1 ← M[r2+5] |
| sw | 100 | I | sw r1 r2 3 | r1 →M[r2+3] |
| and | 101 | R | and r1 r2 r3 | r1 = r2 && r3 |
| xor | 110 | R | xor r1 r2 r3 | r1= r2 xor r3 |
| j | 111 | J | j 5 | Jump to PC=5 |